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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,629	MORRISON ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 19, 2005 has been entered. Claims 21-29 are now pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

At the outset, it is noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981) and *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant contends that the system of Lee is not a cellular system at either the hardware or virtual machine levels, and that even if it were, Lee fails to disclose separate physical management and high-speed interconnects, and cells each having management processors (remarks, page 9, third full paragraph).

However, Applicant acknowledges that Lee discloses a physical bus, a separate physical management interconnect and a physical management processor (remarks, pages 8-9, bridging paragraph). Indeed, these hardware elements are partitioned into logical partitions or logical "cells" in the system (see, for example, partitioned hardware 230 in FIG. 2 and column 5, lines

32-39). In Lee, FIGS. 1-3 are simply different views of the same system, or as Applicant indicates, different levels of the same architecture (remarks, page 8, last full paragraph). Regardless of which elements Lee describes with reference to any given view of the system, the physical bus, the separate physical management interconnect and the physical management processor are each present in the system as a whole. Lee's system is considered a "cellular" system in the sense that it is partitioned into logical partitions or cells, as noted above. Each logical cell comprises physical elements at the hardware level.

For example, Lee discloses a situation in which the system is partitioned into three cells, each having one or more processors, memories and I/O adapters (see, for example, column 3, lines 35-45), and each having a separate operating system (see, for example, column 3, lines 46-57). The physical bus and the separate physical management interconnect are necessarily part of each logical cell (see, for example, system bus 106 and JTAG/I^2C buses 134 in FIG. 1), and likewise, each logical cell uses the physical management processor (see, for example, column 4, lines 41-53, and column 4, line 61 to column 5, line 7). Thus, each logical cell is considered to comprise a physical management processor.

Applicant acknowledges that the system of Goodman is a cellular system at the hardware level, and that Goodman discloses many of the elements that Applicant contends are missing in Lee (remarks, page 9, last two paragraphs). Applicant contends that Goodman does not disclose management processors and management interconnects (remarks, page 10, first paragraph). Regardless, these hardware elements are disclosed in Lee, as noted above. Similarly, Applicant acknowledges that Forsman discloses a service processor, but contends that Forsman's machine

is not a cellular machine (remarks, page 10, fourth and fifth paragraphs). However, Lee and Goodman disclose cellular systems, as noted above.

From the arguments above, Applicant concludes that the cited combination of references fails to provide elements recited in independent claim 21 (remarks, pages 10-11, bridging paragraph), and that the cited combination of references fails to provide the hardware-level or physical-level management interconnects and cellular management processors recited in independent claim 27 (remarks, page 11, first full paragraph).

However, the examiner does not agree with Applicant's conclusion. Applicant's arguments are addressed above, and the language of claims is addressed below.

Similarly, Applicant contends that Lee fails to disclose cells at the sole level of architecture where the management interconnect exists, that Forsman discloses only one interconnect, and that Goodman fails to disclose a management interconnect that is distinct from a high-speed interconnect (remarks, page 11, middle paragraphs).

However, as noted above, Lee's management interconnect does indeed exist in the system, regardless of which view or which level of the system is illustrated. Each logical partition or cell necessarily incorporates the management interconnect.

The examiner would suggest that Applicant focus on the crux of the invention, perhaps such as the manner in which the firmware is updated, rather than on the arrangement of hardware in the system. It is noted that conventional NUMA systems are known to comprise cells at the hardware level that are interconnected with separate high-speed and slow-speed interconnects, wherein each cell includes one or more processors and local memories, a manageability system

processor, and a nonvolatile memory with firmware stored therein, as admitted in Applicant's specification (see the background of the invention, pages 1-2).

Double Patenting

3. The provisional obviousness-type double patenting rejection is withdrawn in view of the abandonment of the conflicting Application No. 09/998,630 (see Applicant's remarks, page 7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,834,340 to Lee et al. (art of record, "Lee") in view of U.S. Pub. No. 2002/0091807 to Goodman (art of record, "Goodman") in view of U.S. Pat. No. 6,665,813 to Forsman et al. (art of record, "Forsman").

With respect to claim 21 (currently amended), Lee discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, the abstract), the system comprising:

(a) a physical high speed interconnect (see, for example, system bus 106 in FIG. 1);

(b) a first cell and a second cell, each cell comprising at least one processor coupled to at least one random-access memory subsystem, at least one nonvolatile memory system, and a

high-speed interconnect interface (see, for example, FIG. 2 and column 5, lines 32-39, which shows a plurality of logical partitions or cells that each comprise at least one processor coupled to at least one random-access memory and a nonvolatile memory, and see, for example, FIG. 1, which further shows that each processor is coupled to the high-speed interconnect);

(c) wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, FIG. 1, which shows that each processor is coupled to the high-speed interconnect).

Lee discloses testing the cells to detect and recognize errors (see, for example, column 4, lines 41-53), and further discloses updating the firmware (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitations:

(d) wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

(e) wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware; and

(f) wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell.

However, in an analogous cellular computer system, Goodman discloses updating the firmware recorded in the nonvolatile memories of the nodes or cells in the system (see, for example, FIG. 1 and the abstract).

Goodman discloses a first cell that has outdated firmware (see, for example, paragraph 0021, lines 1-9 and 16-18), and a second cell that has valid firmware (see, for example, paragraph 0021, lines 10-15), as in part (d) above.

Goodman further discloses that the first cell has code to determine that its firmware is outdated (see, for example, paragraph 0025, lines 2-13) and to update the first cell with firmware copied from a cell that has valid firmware (see, for example, paragraph 0027, lines 10-13), as in part (e) above.

Goodman further discloses that the second cell has code to determine that its firmware is valid (see, for example, paragraph 0023, lines 7-14) and to transmit its firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (f) above.

Goodman discloses that updating the firmware in the above manner increases the likelihood that each node or cell in the system will have the same version of the firmware, so as to prevent incompatibility problems due to different firmware levels in different cells (see, for example, paragraph 0010, lines 8-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee with the firmware update features of Goodman, so as to increase the likelihood that each partition or cell will have the same version of firmware and thus prevent incompatibility problems.

Lee in view of Goodman does not expressly disclose that the outdated firmware is corrupt firmware.

However, Forsman discloses updating firmware and recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55). Forsman further discloses recovering the firmware if the update is corrupt (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee in view of Goodman so as to recognize whether the firmware is corrupt, such as in Forsman, so that the firmware can be updated and recovered if needed.

With respect to claim 22 (currently amended), the rejection of claim 21 is incorporated, and Lee further discloses:

(a) a physical manageability system interconnect (see, for example, JTAG/I^2C buses 134 in FIG. 1);

(b) wherein the first cell and second cell each further comprise a management processor (see, for example, service processor 135 in FIG. 1).

Lee discloses testing the cells to detect and recognize errors using the management interconnect (see, for example, column 4, lines 41-53), and further discloses updating the firmware based on a flash request and an acknowledgement from one of the cells (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitation:

(c) wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, to enable the high

speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

However, Goodman further discloses that the second cell has code to receive a request for valid firmware and to transmit an acknowledgement in response (see, for example, paragraph 0023, lines 7-14), to enable the interconnect (see, for example, paragraph 0017, lines 14-21), and to transmit the firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (c) above.

With respect to claim 23 (currently amended), the rejection of claim 21 is incorporated, and Lee further discloses:

(a) a manageability system interconnect (see, for example, JTAG/I^2C buses 134 in FIG. 1);

(b) wherein the first cell and second cell further comprise a management processor (see, for example, service processor 135 in FIG. 1).

Lee discloses testing the cells to detect and recognize errors using the management interconnect (see, for example, column 4, lines 41-53), and further discloses updating the firmware based on a flash request and an acknowledgement from one of the cells (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitation:

(c) wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.

However, Goodman further discloses that the second cell has code to receive a request for valid firmware and to transmit an acknowledgement in response (see, for example, paragraph 0023, lines 7-14), and to transmit the firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (c) above.

With respect to claim 24 (new), Lee discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, the abstract), the system comprising:

(a) a high speed interconnect (see, for example, system bus 106 in FIG. 1);

(b) a first cell and a second cell, each cell comprising at hardware level: at least one processor of the cell coupled to at least one random-access memory subsystem of the cell, at least one nonvolatile memory system coupled to the at least one processor of the cell, a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect (see, for example, FIG. 2 and column 5, lines 32-39, which shows a plurality of logical partitions or cells that each comprise at least one processor coupled to at least one random-access memory and a nonvolatile memory, and see, for example, FIG. 1, which further shows that each processor is coupled to the high-speed interconnect),

(c) wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, FIG. 1, which shows that each processor is coupled to the high-speed interconnect).

Lee discloses testing the cells to detect and recognize errors (see, for example, column 4, lines 41-53), and further discloses updating the firmware (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitations:

(d) wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

(e) wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware; and

(f) wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell.

However, in an analogous cellular computer system, Goodman discloses updating the firmware recorded in the nonvolatile memories of the nodes or cells in the system (see, for example, FIG. 1 and the abstract).

Goodman discloses a first cell that has outdated firmware (see, for example, paragraph 0021, lines 1-9 and 16-18), and a second cell that has valid firmware (see, for example, paragraph 0021, lines 10-15), as in part (d) above.

Goodman further discloses that the first cell has code to determine that its firmware is outdated (see, for example, paragraph 0025, lines 2-13) and to update the first cell with firmware copied from a cell that has valid firmware (see, for example, paragraph 0027, lines 10-13), as in part (e) above.

Goodman further discloses that the second cell has code to determine that its firmware is valid (see, for example, paragraph 0023, lines 7-14) and to transmit its firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (f) above.

Goodman discloses that updating the firmware in the above manner increases the likelihood that each node or cell in the system will have the same version of the firmware, so as to prevent incompatibility problems due to different firmware levels in different cells (see, for example, paragraph 0010, lines 8-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee with the firmware update features of Goodman, so as to increase the likelihood that each partition or cell will have the same version of firmware and thus prevent incompatibility problems.

Lee in view of Goodman does not expressly disclose that the outdated firmware is corrupt firmware.

However, Forsman discloses updating firmware and recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55). Forsman further discloses recovering the firmware if the update is corrupt (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee in view of Goodman so as to recognize whether the firmware is corrupt, such as in Forsman, so that the firmware can be updated and recovered if needed.

With respect to claim 25 (new), the rejection of claim 24 is incorporated, and Lee further discloses:

(a) a manageability system interconnect (see, for example, JTAG/I^2C buses 134 in FIG. 1);

(b) wherein the first cell and second cell further comprise at hardware level a management processor (see, for example, service processor 135 in FIG. 1).

Lee discloses testing the cells to detect and recognize errors using the management interconnect (see, for example, column 4, lines 41-53), and further discloses updating the firmware based on a flash request and an acknowledgement from one of the cells (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitation:

(c) wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

However, Goodman further discloses that the second cell has code to receive a request for valid firmware and to transmit an acknowledgement in response (see, for example, paragraph 0023, lines 7-14), to enable the interconnect (see, for example, paragraph 0017, lines 14-21), and to transmit the firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (c) above.

With respect to claim 26 (new), the rejection of claim 24 is incorporated, and Lee further discloses:

(a) a manageability system interconnect (see, for example, JTAG/I^2C buses 134 in FIG. 1);

(b) wherein the first cell and second cell further comprise a management processor (see, for example, service processor 135 in FIG. 1).

Lee discloses testing the cells to detect and recognize errors using the management interconnect (see, for example, column 4, lines 41-53), and further discloses updating the firmware based on a flash request and an acknowledgement from one of the cells (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitation:

(c) wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.

However, Goodman further discloses that the second cell has code to receive a request for valid firmware and to transmit an acknowledgement in response (see, for example, paragraph 0023, lines 7-14), and to transmit the firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (c) above.

6. Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Goodman.

With respect to claim 27 (new), Lee discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, the abstract), the system comprising:

(a) a high speed interconnect (see, for example, system bus 106 in FIG. 1);

(b) a management interconnect (see, for example, JTAG/I^2C buses 134 in FIG. 1);

(c) a first cell and a second cell, each cell comprising at hardware level: at least one processor of the cell coupled to at least one random-access memory subsystem of the cell, at least one nonvolatile memory system coupled to the at least one processor of the cell, a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect (see, for example, FIG. 2 and column 5, lines 32-39, which shows a plurality of logical partitions or cells that each comprise at least one processor coupled to at least one random-access memory and a nonvolatile memory, and see, for example, FIG. 1, which further shows that each processor is coupled to the high-speed interconnect), a management processor of the cell coupled to a nonvolatile memory for management code of the cell, and an interface coupling the management processor of the cell to the management interconnect (see, for example, service processor 135 and nonvolatile memory 192 in FIG. 1);

Lee discloses testing the cells to detect and recognize errors using the management interconnect (see, for example, column 4, lines 41-53), and further discloses updating the firmware based on a flash request and an acknowledgement from one of the cells (see, for example, FIG. 4 and column 6, lines 32-65), but does not expressly disclose the limitations:

(d) wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware selected from the group consisting of outdated or corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

(e) wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware and, upon recognizing that the firmware of the first cell is errored, for transmitting over the management

interconnect a request for valid firmware to the second cell, and for updating the nonvolatile memory system of the first cell with valid firmware;

(f) wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell; and

(g) wherein the management code of the second cell comprises machine readable code to receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.

However, in an analogous cellular computer system, Goodman discloses updating the firmware recorded in the nonvolatile memories of the nodes or cells in the system (see, for example, FIG. 1 and the abstract).

Goodman discloses a first cell that has outdated firmware (see, for example, paragraph 0021, lines 1-9 and 16-18), and a second cell that has valid firmware (see, for example, paragraph 0021, lines 10-15), as in part (d) above.

Goodman further discloses that the first cell has code to determine that its firmware is outdated (see, for example, paragraph 0025, lines 2-13), to transmit a request for the valid firmware to the second cell (see, for example, paragraph 0027, lines 3-6), and to update the first cell with the valid firmware (see, for example, paragraph 0027, lines 10-13), as in part (e) above.

Goodman further discloses that the second cell has code to determine that its firmware is valid (see, for example, paragraph 0023, lines 7-14) and to transmit its firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (f) above.

Goodman further discloses that the second cell has code to receive a request for valid firmware and to transmit an acknowledgement in response (see, for example, paragraph 0023, lines 7-14), to enable the interconnect (see, for example, paragraph 0017, lines 14-21), and to transmit the firmware to the first cell (see, for example, paragraph 0027, lines 6-8), as in part (g) above.

Goodman discloses that updating the firmware in the above manner increases the likelihood that each node or cell in the system will have the same version of the firmware, so as to prevent incompatibility problems due to different firmware levels in different cells (see, for example, paragraph 0010, lines 8-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee with the firmware update features of Goodman, so as to increase the likelihood that each partition or cell will have the same version of firmware and thus prevent incompatibility problems.

With respect to claim 29 (new), the rejection of claim 27 is incorporated, and Goodman further discloses the limitation wherein the errored firmware is outdated firmware (see the rejection of claim 27 above).

7. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Goodman, as applied to claim 27 above, and further in view of Forsman.

With respect to claim 28 (new), the rejection of claim 27 is incorporated, and Lee in view of Goodman does not expressly disclose the limitation wherein the errored firmware is corrupt firmware.

However, Forsman discloses updating firmware and recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55). Forsman further discloses recovering the firmware if the update is corrupt (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Lee in view of Goodman so as to recognize whether the firmware is corrupt, such as in Forsman, so that the firmware can be updated and recovered if needed.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2192

mjy

TUAN DAM
SUPERVISORY PATENT EXAMINER